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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,875	06/20/2003	Blaine Stackhouse	200207083-1	6673

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EXAMINER	
NGUYEN, DANG T	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/600,875	STACKHOUSE ET AL.	
	Examiner	Art Unit	
	Dang T. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-20* is/are allowed.

6)☒ Claim(s) *1,3-8,11 and 21-25* is/are rejected.

7)☒ Claim(s) *2,9,and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search history*.

Response to Amendment

1. This office action is in response to applicant's amendment received on 3/28/05. Claim 1 has been amended. Claims 1 - 25 are pending on this application. Claims 1, 6, 12, 17, and 21 are independent claims.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-8, 11, and 21-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Urakami et al. U.S. patent No. 6,794,909 B1 – filed August 21, 2003.

Regarding independent claim 1, Fig. 3 of Urakami et al. discloses a bias generator (11, although Urakami et al. does not discloses 11 is a bias generator, however the output signal OUTPUT of 11 must providing a bias level to other circuit *see fig.1[5]* therefore 11 is a bias generating circuit) for testing (Col. 7 lines 23 – 29) of a static random access memory SRAM (Col. 1 line 19) comprising: an output of the bias generator (output node of 11) and means (14) for adjusting a set of available magnitudes at the output of a bias voltage output signal (Col. 5 lines 8 – 26) at the output using metal programming (Although Urakami et al. does not explicit discloses the adjusting means 14 is a metal programming, however the programming transistors 27

and 28 discloses in 11 of Urakami are P type and N type metal-oxide transistors and having the same type transistor of applicant's disclosure. Therefore the transistor 27 and 28 must be metal programming transistors)

Regarding dependent claim 3, Fig. 2 of Urakami discloses wherein the means for adjusting (14) comprises a metal transistor (27, 28) in the bias generator (Fig. 2), the metal programmable transistor (27, 28) comprising either or both of a metal-programmable pull-up transistor and a metal-programmable pull-down transistor that change one or both of a range and a resolution of the set of available magnitudes when the metal-programmable transistor is metal programmed (Col. 5 lines 8 – 26).

Regarding dependent claim 4, Fig. 2 of Urakami discloses further comprising: a pull-up array of transistors (27) connected between a first supply voltage (Vdd) and the bias generator output (OUTPUT); a pull-down transistor (28) connected between the bias generator output (OUTPUT) and a second supply voltage (GROUND); and a gate bias circuit (15, 18) connected between a mode select input (12, 13) and a gate of the pull-down transistor (28), wherein the metal-programmable pull-up transistor (27) is connectable in parallel or in series with the pull-up transistor array, and wherein the metal-programmable pull-down transistor (28) is connectable in parallel or in series with the pull-down transistor (14).

Regarding dependent claim 5, Fig. 2 of Urakami discloses wherein each of the metal-programmable pull-up transistor and the metal-programmable pull-down transistor (27, 28) has a respective ON state resistance that, when either or both are metal programmed, combines with an effective ON state resistance of the pull-up transistor

array and an ON state resistance of the pull-down transistor (19 – 21) to adjust the set of available magnitudes (Col. 5 lines 8 – 26).

Regarding dependent claim 6, Fig. 3 of Urakami et al. discloses a bias generator (11) for testing (Col. 7 lines 23 – 29) of a static random access memory SRAM ((Col. 1 line 19)) comprising: a metal programmable transistor (14) that adjusts a set of available magnitudes (Col. 5 lines 8 – 26) of a bias voltage output signal (11) at the bias generator output (OUTPUT) when metal programmed (Col. 5 lines 8 – 26).

Regarding dependent claims 7 and 8, the claims incorporated the same subject matter as of claims 3 and 4, and rejected along the same rationale.

Regarding dependent claim 11, Fig. 2 of Urakami discloses wherein the pull-up array transistors are p- type metal oxide semiconductor (27) transistors that function to pull up the bias voltage output signal when in an ON state, and wherein the pull-down transistor is an n-type metal oxide semiconductor (28) transistor that functions to pull down the bias voltage output signal to the second supply voltage (Ground) when in the ON state, the second supply voltage being less than the first supply voltage, the second supply voltage optionally being zero volts or a ground voltage (Ground).

Regarding dependent claim 21, Fig. 3 of Urakami discloses a method of modifying a set of available magnitudes (Col. 5 lines 8 – 26) of a bias voltage output signal (OUTPUT) generated by a bias generator comprising (11): providing a metal-programmable transistor (27, 28) in the bias generator (11); and metal programming (Ø1, Ø2, Øn) the metal-programmable transistor (27, 28) to connect the transistor to circuitry of the bias generator (11), such that a corresponding ON state resistance of the

metal-programmed transistor (27, 28) is combined with an effective ON state resistance of the circuitry (11) to modify the available magnitudes of the set (Col. 5 lines 8 – 26).

Regarding dependent claims 22 - 24, the claims incorporated substantial the same subject matter as of claims 3 and 4, and rejected along the same rationale.

Regarding dependent claim 25, Fig. 2 of Urakami discloses wherein providing a metal programmable transistors (14) comprises providing either or both of a selection of metal-programmable pull-up transistors (27) and a selection (13, Ø1, Ø2, Øn) of metal-programmable pull-down transistors in the bias generator (Fig. 2), at least one (27.1) of the metal-programmable transistors of each respective selection (Ø1, Ø2, Øn) being different from other metal-programmable transistors (27.2, 27.3, 27.n) of the respective selections (Ø1, Ø2, Øn), and wherein metal programming the metal-programmable transistor (27, 28) comprises selecting (12, 13, Ø1, Ø2, Øn) a respective metal-programmable transistor (27, 28) from either or both the pull-up transistor selection and the pull-down transistor selection, and connecting the selected Ø1, Ø2, Øn respective metal-programmable transistor to the bias generator circuitry (OUTPUT).

Allowable Subject Matter

3. Claims 2, 9 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 2, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest " wherein the bias voltage output

signal biases a gate of a weak write pull-down transistor of a write drives in the SRAM with a target magnitude predetermined for the SRAM".

With respect to claims 9 and 10 the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "wherein the mode select input controls a selection between a weak write test mode (WWTM) and a default mode of operation of the bias generator, a set of selection inputs selecting the set of available magnitudes of the bias voltage output signal in the WWTM, the bias voltage output signal being a logic high level at the bias generator output in the default mode.".

4. Claims 12 – 20 are allowed over prior art.

The following is a statement of reasons for the indication of allowable subject matter:

With regard to claims 12 and 17, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "a bias generator having a first transistor having a source connected to drains of the pull-up transistor array, a drain connected to the bias generator output and a gate connected to an inverse mode select input; and a second transistor having a source connected to the second supply voltage, a drain connected to the bias generator output, and a gate connected to the inverse mode select input, wherein the mode select input and the inverse mode select input control a selection between a weak write test mode (WWTM) and a default mode of operation of the bias generator, a set of selection inputs selecting the set of available magnitudes of the bias voltage output signal in the WWTM, the bias voltage output signal being a logic low level at the bias generator output in the default mode".

Response to Arguments

5. Applicant's arguments with respect to claims 1, 6 and 21 have been considered but are moot in view of the new ground(s) of rejection.

Prior art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Beffa et al.	Patent No.: 6,094734	Date of Patent: Jul. 25, 2000
Hsueh et al.	Patent No.: 5,179,297	Date of Patent: Jan. 12, 1993

Contact Information

7. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the

patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 5/13/2005

ANH PHUNG
PRIMARY EXAMINER